Ambipolar pentacene/C_{60}-based field-effect transistors with high hole and electron mobilities in ambient atmosphere

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Ambipolar field-effect transistors (FETs) were fabricated with a heterostructure of pentacene/C_{60} in which the C_{60} layer functioned as an n-type channel while the pentacene layer functioned as both a p-type channel and a sealing capsule for the unstable C_{60} layer. The ambipolar FET, operating in an ambient atmosphere, exhibited a hole mobility of 0.2 cm^{2}/Vs with a threshold voltage of −2.3 V and an electron mobility of 0.04 cm^{2}/Vs with a threshold voltage of 66 V with moderately good air stability. However, the threshold voltage and gate voltage for the n-channel operation must be improved for practical applications. © 2009 American Institute of Physics.

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Organic field-effect transistors (OFETs) have attracted great attention for potential applications as flexible structures, with large integrated areas, due to their low cost processing. Among OFETs, ambipolar OFETs have become research targets since they are potentially available for complementary-metal-oxide-semiconductor (CMOS) inverters with ease of design and fabrication. Pentacene is stable in ambient atmosphere and FETs with a thin film of pentacene exhibited the highest hole mobility (~1.5 cm^{2}/Vs) among air-stable p-channel organic semiconductors. On the other hand, C_{60} is a well-known semiconductor, however, are believed to require a self-assembled monolayer (SAM) of an organic compound such as octadecyltrichlorosilane (OTS) or hexamethyldisilazane on the SiO_{2} surface before deposition of pentacene in order to obtain higher performance of the pentacene FETs. Such improvement of the FET performance is considered to be due to the optimization of homogeneous coverage or grain size of the pentacene on the SAM-formed SiO_{2} surface during deposition. From this, we can extrapolate that optimization of the pentacene surface layer before C_{60} deposition may improve the C_{60} grain size and the electron mobility.

Kuwahara et al. reported fabrication of an ambipolar OFET with a heterostructure of C_{60} and pentacene, showing a hole mobility of 6.8 × 10^{-2} cm^{2}/Vs in p-channel operation and an electron mobility of 1.3 × 10^{-2} cm^{2}/Vs in n-channel operation, measured in a vacuum. These ambipolar characteristics, however, appeared only after annealing at 80–120 °C for 24 h under 10^{-6} Torr. Cosseddu et al. fabricated an all-organic ambipolar FET with a heterostructure of C_{60} and pentacene, operating in air atmosphere, showing a hole mobility of 1.0 × 10^{-2} cm^{2}/Vs and an electron mobility of 3.5 × 10^{-4} cm^{2}/Vs. Although the result is significant in terms of all-organic flexible devices, the electron mobility in the n-channel of C_{60} is too low to use in CMOS inverters. The low electron mobility is most likely due to the instability of C_{60} in air atmosphere during n-channel operation. This result also indicates that C_{60}-based FETs with high mobility for operation under ambient atmosphere may require encapsulation.

On the other hand, Itaka et al. proposed that a pentacene buffer layer optimized the crystallization or grain size of the C_{60} deposited on the buffer layer due to the “molecular wetting” effect. Indeed they claimed the highest electron mobility of 4.9 cm^{2}/Vs of C_{60} by such an approach, although an ultraflat surface of sapphire was used as the base substrate. They found that pentacene formed a monolayer during deposition by a combinatorial molecular beam epitaxy method. Conventional SiO_{2}/Si wafers used in OFET studies, however, are believed to require a self-assembled monolayer (SAM) of an organic compound such as octadecyltrichlorosilane (OTS) or hexamethyldisilazane on the SiO_{2} surface before deposition of pentacene in order to obtain higher performance of the pentacene FETs. Such improvement of the FET performance is considered to be due to the optimization of homogeneous coverage or grain size of the pentacene on the SAM-formed SiO_{2} surface during deposition. From this, we can extrapolate that optimization of the pentacene surface layer before C_{60} deposition may improve the C_{60} grain size and the electron mobility.

In this letter, we present the fabrication of OFETs with a heterostructure of pentacene/C_{60} in which the C_{60} layer functions as an n-type channel, while the pentacene layer functions as both a p-type channel and a sealing capsule for the unstable C_{60} layer. The self-encapsulated ambipolar FET, operating in an ambient atmosphere, exhibited a hole mobility of 0.2 cm^{2}/Vs in the p-type operation and an electron mobility of 0.04 cm^{2}/Vs in the n-type operation, with moderately good air stability.

We fabricated the ambipolar FET channels by utilizing poly(3,4-ethylenedioxythiophene) / poly(4-styrenesulfonate) (denoted as PEDOT/PSS) microfibers, similar to a procedure previously reported by us. The PEDOT/PSS microfibers were fabricated by a wet-spinning technique. A typical fabrication procedure for a pentacene/C_{60}/pentacene FET with top-contact configuration is as follows. About 1 ml of PEDOT/PSS dispersion solution was poured into a glass cylinder and extruded into a coagulation bath containing acetone by a single-hole spinneret, resulting in a microfiber. The microfiber was carefully loaded on graph paper and dried in vacuum at 160 °C for 1 h before used as a channel mask. A heavily doped n-type silicon wafer with a SiO_{2} thin layer (350 nm) was washed in pure water and acetone and ultraviolet (UV) light-ozone treatment was carried out in order to remove organic contaminants. Next, an OTS-SAM was prepared on the UV-ozone treated substrate by the im-
To easily remove, resulting in the channel pattern to complete the microfiber as the channel mask. The microfiber was then mersing method. Active layers were deposited in three steps. First, a 5-nm-thick pentacene layer was thermally deposited on the SAM-formed substrate as a buffer layer for the $C_{60}$ layer. Second, a 30-nm-thick $C_{60}$ layer was deposited without breaking the vacuum. Finally, a 30-nm-thick pentacene layer was deposited with a wider mask in order to completely encapsulate the deposited $C_{60}$ layer. Gold was thermally deposited in vacuum on the top pentacene layer using the microfiber as the channel mask. The microfiber was then easily removed, resulting in the channel pattern to complete the fabrication of the top-contacted ambipolar OFET (see Fig. 1). The patterned channel length was evaluated by scanning electron microscopy (SEM). The output characteristics were measured with a semiconductor parameter analyzer (4200-SCS Keithley) and the hole and electron mobilities were calculated from the saturation regimes\[^{11}\] of $p$- and $n$-channel operations, respectively, in ambient atmosphere under simple nitrogen flow. After measuring the electrical characteristics, a cross section of the device was created by a microtome and observed by scanning transmission electron microscopy (STEM).

The pentacene/$C_{60}$-based FET with $L/W$ of 1.2/1000 $\mu$m measured by a top-viewed SEM image (Fig. 2) of the device, showed saturation of the hole drain current at gate voltages from 0 to $-50$ V and a threshold voltage ($V_T$) of $\approx -2.3$ V during $p$-channel operation, as shown in Fig. 3 (left). On the other hand, the FET showed saturation of the electron drain current at gate voltages of 40--100 V and a threshold voltage ($V_T$) of 66 V during $n$-channel operation, as shown in Fig. 3 (right). We evaluated the FET mobilities of the ambipolar OFETs using the dielectric constant and thickness values of the $SiO_2$ ($\varepsilon_r=3.9$ and $d=350$ nm). The hole mobility was estimated to be $0.2$ cm$^2$/V s during $p$-channel operation and the electron mobility was $0.04$ cm$^2$/V s during $n$-channel operation. It should be noted that both hole mobility and electron mobility observed in an ambient atmosphere were the highest among the reported ambipolar pentacene/$C_{60}$ FETs.\[^{6}\] After storing the ambipolar device under slightly reduced pressure for 6 days, we measured the output characteristics again, as shown in Fig. 4. Surprisingly, the mobilities of both hole and electron were 0.2 and 0.01 cm$^2$/V s, respectively, indicating reasonable stability for the $p$-channel operation and moderately good stability for the $n$-channel operation. This device is also the first air-stable pentacene/$C_{60}$ ambipolar FET with such high electron mobility. However, the threshold voltage and gate voltage for the $n$-channel operation were as high as 66 and 100 V, respectively, which may make it difficult to use current devices directly in CMOS inverters.

Cross-sectional STEM images clearly show the bottom pentacene layer, middle $C_{60}$ layer, and top pentacene layer (Fig. 5). Energy dispersive x-ray (EDX) spectra show that the three layers contained mainly carbon elements. The thickness was, however, inhomogeneous and different values were measured by a thermal deposition instrument equipped with a quartz crystal microbalance. As mentioned, the thick top layer of pentacene (30 nm) is considered to function as both $p$-channel and sealing capsule. The thickness of the top layer would be reduced if the deposition conditions of the $C_{60}$ were optimized to result in a homogeneous thin layer.

Kuwahara et al.\[^{12}\] investigated the thickness of the pentacene layer under the $C_{60}$ layer in terms of mobilities. When the thickness of the pentacene layer was larger than 25 nm, the hole mobility of the ambipolar pentacene/$C_{60}$ FET was as high as $\sim 10^{-1}$ cm$^2$/V s. The hole mobility, however,
sharply decreased when the thickness was less than 25 nm, decreasing to $10^{-4}$ cm$^2$/V s when the thickness was 10 nm. Therefore, in the present ambipolar pentacene/C$_{60}$/pentacene FET, which exhibited a high mobility of 0.2 cm$^2$/V s, the top pentacene layer with thickness of 30 nm must function as the $p$-channel, rather than the bottom pentacene layer with thickness of 5 nm.

We also ran preliminary investigations on the top pentacene layer in terms of protection of the C$_{60}$ layer from air. In several trials, no $n$-channel characteristics were observed for devices without the top pentacene layer. Accordingly, we considered that the top pentacene layer also functions as a protecting layer for the air-sensitive C$_{60}$ layer.

In summary, we fabricated ambipolar FETs with a heterostructure of pentacene/C$_{60}$/pentacene in which the C$_{60}$ layer functioned as an $n$-type channel, while the pentacene layer functioned as both a $p$-type channel and a sealing capsule for the unstable C$_{60}$ layer. The self-encapsulated ambipolar FET, operating in an ambient atmosphere, exhibited a hole mobility of 0.2 cm$^2$/V s with $V_T$ of $-2.3$ V in $p$-channel operation and an electron mobility of 0.04 cm$^2$/V s with $V_T$ of 66 V in $n$-channel operation, with moderately good air stability. It is significant that simultaneous self-encapsulation with a stable $p$-channel layer may simplify the fabrication process of C$_{60}$-based ambipolar FETs. It is believed that more suitable sealing materials would further improve the performance of the devices.

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